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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,433	03/25/2005	Yoshinori Toumiya	09792909-6196	6644

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/529,433	TOUMIYA, YOSHINORI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The preliminary amendment filed on 3/25/05 has been entered.

Election/Restriction

2. Applicant's election without traverse of the group I invention, claims 12-22, in the reply filed on 10/11/06 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 3/25/05 is acceptable.

Drawings

4. The formal drawings filed on 3/25/05 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 3/25/05 has been considered.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"said intra-lens," "the uppermost layer wirings," "said intra-lenses," and "said wirings" have no antecedent basis.

Correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 12,13,16,17, and 19-21 are rejected under 35 U.S.C. 102(a) as being anticipated by TANAKA (JP-2002110953), as cited by applicant on 3/25/2005.

A. With regard to claims 12 and 13 Tanaka discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming a plurality of light-receiving portions 102 on the surface of a substrate 101; forming wirings 106-107 on both sides of

each of said light-receiving portions 102; forming a first insulation layer 109 having a first refractive index n2; etching said first insulation layer 109 by using an etching mask 201 and forming a concave portion 111 above each of said light-receiving portions 102; and forming a second insulation layer 110 with a second refractive index n3 to bury said concave portion 111; and prior to the step of forming said wirings 106-107, forming a charge readout transistor 103; forming a gate electrode 104 to operate said charge readout transistor 103; and forming a planarizing film 105 which covers said gate electrode 104, wherein said wirings 106-107 and said concave portion 111s are formed above said planarizing film 105. Note figures 1 and 2 and paragraphs 0020-0030 of Tanaka.

B. With regard to claims 16,17,19, and 20, Tanaka discloses a solid-state imaging device comprising a plurality of pixels arranged each including a light-receiving portion 102 and a MOS transistor 103, uppermost metallic Al layer wirings 106-107 positioned on both sides of said light-receiving portion 102 and asymmetrically disposed with respect to said light-receiving portion 102, and a single intra-layer lens formed without being affected by said asymmetrical uppermost wirings 106-107 and corresponding to each of said light-receiving portions 102. Note figure 1 and paragraphs 0020-0030 of Tanaka.

C. With regard to claim 21 Tanaka discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming wirings 106-107 on a semiconductor region 101 in which a plurality of pixels each including a light-receiving portion 102 and a MOS transistor 103 are arranged through an insulation layer 105 with

the light-receiving portion 102 in between; forming a first insulation layer 109 with a first refractive index n2 across the whole surface thereof; selectively removing said first insulation layer 109 with a etching mask 201 by isotropic-etching at a position corresponding to said light-receiving portion 102 to form a concave portion 111 corresponding to each light-receiving portion 102; forming a second insulation layer 110 with a second refractive index n3 across the whole surface including said concave portion 111; and planarizing said second insulation layer 110 and making the second insulation layer 110 remain within said concave portion 111 to form a single intra-lens using said first 109 and second 110 insulation layers. Note figures 1 and 2 and paragraphs 0020-0030 of Tanaka.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 15, and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over TANAKA (JP-2002110953) in view of MATSUDA ET AL. (JP11-40787).

With regard to claims 14 and 15 Tanaka discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming a plurality of light-receiving portions 102 on the surface of a substrate 101; forming wirings 106-107 on both sides of

each of said light-receiving portions 102; forming a first insulation layer 109 with a first refractive index n2; etching back said first insulation layer 109; and forming a second insulation layer 110 with a second refractive index n3 on said first insulation layer 109; and forming a third insulation layer 105 to cover said convex surface of said first insulation layer 109 prior to the step of forming said second insulation layer 110. Note figures 1 and 2 and paragraphs 0020-0030 of Tanaka. Tanaka does not disclose the steps of forming a reflow film with a convexly curved surface at a position corresponding to the respective light-receiving portions and etching back said reflow film with the first insulation layer to transfer said convexly curved surface onto the first insulation layer.

However, Matsuda et al. discloses a method for manufacturing a solid-state imaging device comprising, inter alia, the steps of forming a reflow film 7 with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film 7 with a first insulation layer 6 to transfer said convexly curved surface onto the first insulation layer 6. Note figure 2 and paragraphs 0016-0020 of Matsuda et al. Therefore, it would have been obvious to a person having skill in the art to augment Tanaka's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. in order to form the interlayer lens in a desired shape to thus improve condensing efficiency.

With regard to claim 22 Tanaka discloses a method for manufacturing a solid-state imaging device comprising the steps of: forming wirings 106-107 on a semiconductor

region 101 in which a plurality of pixels each including a light-receiving portion 102 and a MOS transistor 103 are arranged through an insulation layer 105 with the light-receiving portion 102 in between; forming a first insulation layer 109 with a first refractive index n2 across the whole surface thereof; etching back said first insulation layer 109; and forming a planarizing film 105 with a second refractive index n3 on said first insulation layer 109 to form a single intra-layer lens including said first insulation layer 109 and said planarizing film 105. Note figures 1 and 2 and paragraphs 0020-0030 of Tanaka. Tanaka does not disclose the steps of forming a reflow film with a convexly curved surface at a position corresponding to the respective light-receiving portions and etching back said reflow film with the first insulation layer to transfer said convexly curved surface onto the first insulation layer.

However, Matsuda et al. discloses a method for manufacturing a solid-state imaging device comprising, inter alia, the steps of forming a reflow film 7 with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film 7 with a first insulation layer 6 to transfer said convexly curved surface onto the first insulation layer 6. Note figure 2 and paragraphs 0016-0020 of Matsuda et al. Therefore, it would have been obvious to a person having skill in the art to augment Tanaka's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. in order to form the interlayer lens in a desired shape to thus improve condensing efficiency.

A. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over TANAKA (JP-2002110953) in view of YAMAGUCHI ET AL. (6,344,666).

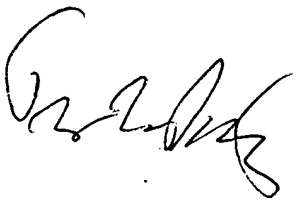
Tanaka discloses a solid-state imaging device comprising a plurality of pixels including all the limitations of claim 18 except the limitation that the center of said intra-layer lens is biased to the center side of an imaging region from the center of said light-receiving portion, when approaching the periphery of the imaging region. Note figure 1 and paragraphs 0020-0030 of Tanaka.

However, Yamaguchi et al. discloses a solid-state imaging device comprising a plurality of pixels including an intra-layer lens 27 whose center is biased to the center side of an imaging region (the imaging region spans the entire imaging device from the center of a light-receiving portion 21, when approaching the periphery of the imaging region. Note figure 2 and column 2 lines 32-39 of Yamaguchi et al. Therefore, it would have been obvious to a person having skill in the art to modify Tanaka's solid-state imaging device by biasing the center of the intra-layer lens to the center side of the imaging region from the center of the light-receiving portion, when approaching the periphery of the imaging region, such as taught by Yamaguchi et al. in order to properly adjust the relative sensitivities of the peripheral and central light-receiving portions, as Yamaguchi et al. explains in column 1 lines 48-67.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisors, Wael M Fahmy (571-272-1705) or Robert J. Pascal (571-272-1769). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Primary Examiner
Art Unit 2826